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Title of Invention	The timing recovery device and the method [Apparatus of timing recovery using interpolation filter] using the interpolation filter.

Abstract

The present invention relates to the timing recovery device and the method using the interpolation filter, and the output signal of A / D (Analog to digital) converter runing with the fixed clock was filtered in the matched filter. After a signal was interpolated by using the interpolation filter, the symbol timing phase difference was detected from the timing error detector. And the coefficient of the interpolation filter was selected in the control circuit than according to the detected symbol timing phase difference as described above and the function of removing the timing phase difference was performed with the coefficient of the interpolation filter. By using a symmetric between the filter factors the filter factor used according to on characteristic time delay of the interpolation filter, the computational complexity and calculation time are reduced by 1/2. In that way the symbol timing of the received signal can be restored in the base band. And the complexity of the interpolation filter structure can be reduced to by 1/2.

Representative Drawing(s)

Fig.

Description

□ Brief Explanation of the Drawing(s)

Figure 1 is a block diagram about the symbol timing recovery apparatus, the process flow chart about the process, where it calculates the interpolation filter output fig. 3 according to the embodiment of the

present invention the structure chart about the interpolation filter which fig. 4 is general, and fig. 5 is the structure chart about the interpolation filter of the present invention of the block diagram about the communications system in which the present invention is applied to, and fig. 2 is the present invention.

#The description of reference numerals of the main elements in drawings#

110: a/D converter 120: fixing frequency clock block.

130: the frequency downward device and matched filter 140: timing recovery circuit.

141: digital interpolation filter 142: the symbol timing recovery apparatus.

150: carrier recovery circuit 151: carrier phase detector.

152: carrier recovery apparatus 160: decision block.

Details of the Invention

Purpose of the Invention

The Technical Field to which the Invention belongs and the Prior Art in that Field

The present invention relates to the timing recovery device and the method using the interpolation filter, particularly, to the timing recovery device and the method when it modulates 4 phase shift method (QPSK) or the signal modulated into the quadrature amplitude modulation (QAM) mode, for restoring the symbol timing of the received signal by using the interpolation filter and timing error detector.

In case of using the digital modem including 4 phase shift method (QPSK:Quaternary Phase Shift Keying) or the quadrature amplitude modulation (QAM:Quadrature Amplituded Modulation) etc. in the radio communications including the high-speed satellite communication, the circuit for restoring the symbol timing if data symbol and sampling point are not synchronized is required. And the method which makes the error signal by directly acting the phase-locked loop (PLL:Phase Locked Loop) on the method for restoring the symbol timing in this way on the sample of the received signal and, corrects the tracing point with the feedback value is very much applied.

For this, conventionally, the method for restoring the symbol timing by using the interpolation filter very much used. The Nyquist (Nyquest) filter was used in the method proposed with especially, the Stephen K/6 as the interpolation filter. And the open loop control mode in which the control signal provided from the symbol timing restructing circuit detected the symbol timing phase difference with the input signal of the interpolation filter and selecting the coefficient group used in the interpolation filter according to the detected symbol phase difference was selected. But in this way, it has the problem a circuit becomes complicated since the implementation of the perfect filter is difficult in the high speed communications of the hundreds Mbps in case of using the Nyquist filter as I interpolation filter in case of using the analog PLL (Phase Locked Loop) or the DPLL (Digdtal PLL) in the cryptanalysis circuit and that the performance degradation can occur. Therefore, it need the implementer for preventing the performance degradation even when ruling out the phase locked loop system in order to implement the symbol timing restructing circuit of the digital method which reduces to a complexity on the circuit implementation while preventing the performance degradation of a system in the high speed communication.

The Technical Challenges of the Invention

Therefore, in the present invention, the raised-cosine (Raised- Cosine) filter is used as the interpolation filter in order to complement the disadvantage. And the timing recovery device and the method which selects the coefficient group of the interpolation filter according to the symbol timing phase difference after nots using PLL and binding the coefficient group of the interpolation filter with a

several and lets the symbol timing location and interpolation filter output out try to be provided.

The control circuit according to the detected symbol timing phase difference as described above the symbol timing phase difference is detected from the timing error detector the timing recovery device which the present invention provides filters the output signal of A / D (Analog to digital) converter runing with the fixed clock in the matched filter, and a signal is interpolated by using the interpolation filter are characterized that the coefficient of the interpolation filter is selected and the function of removing the timing phase difference is performed with the coefficient of the interpolation filter. Moreover, it is characterized that the computational complexity and calculation time are reduced by 1/2 by using a symmetric between the filter factors the filter factor used according to on characteristic time delay of the interpolation filter.

Structure & Operation of the Invention

A below, referring to the figure, the reconstitution device of the present invention and the attached method try to be little more circumstantially illustrated.

Figure 1 is a block diagram about the communications system the present invention being applied to. Referring to Figure 1, it is comprised of the timing recovery circuit (140) performing the timing recovery, the carrier recovery circuit (150) restoring the carrier wave phase difference in the output signal of the timing recovery circuit, and the decision block (160) detecting actually transmitted data in the signal so that the present invention prevent the timing slip generated around the difference of the service clock of a transceiver the frequency downward device and the matched filter (130), for detecting the desired signal and the A/D converter (110) runing with the fixed clock are used so that the applied communications system operate the received signal in the high speed communication, the digital signal transformed with A / D (Analog/Digital) converter (110), converted into the digital signal with the fixing frequency clock (120) operating to the fixed frequency and A/D converter (110) downwardly is directed with frequency. As to the decision block (160), the timing and carrier wave are restored.

At this time, the symbol timing slip is generated due to a difference between the clock used in a receiver and the reference clock which the A/D converter (110) uses in a transmitter because of using the fixed clock. And the interpolation filter in the timing recovery circuit to a need in order to compensate for this.

Moreover, as to the frequency downward device and matched filter (130), after changing the frequency down conversion, and mistake (Real) signal the signal transformed to a digital into the base band into the complex-valued signal of the Q- phase signal and I-phase, it performs the low pass filtering in the matched filter of the parallel configuration. At this time, as to the matched filter part, in the demodulator operating in the high speed, in order to provide the skill of going the frequency down while reducing the computational complexity of a teeth because of being the complicated circuit in which the computational complexity is the greatest and is and, the frequency downward device and matched filter (130) use the matched filter function and the structure at the same time, of accommodating the frequency downward function.

In the meantime, the timing recovery circuit (140) is comprised of the digital interpolation filter (141) and the symbol timing recovery apparatus (142) which is composed of the raised-cosine filter in order to prevent the timing slip generated in the A/D converter (110) and interpolates the output signal of the matched filter (130) and frequency downward device. And it is comprised of the carrier phase detector (151), which the carrier recovery circuit (150) detects the carrier phase in the signal outputted in the digital interpolation filter and the carrier recovery apparatus (152) which again feedbacks the output signal of the carrier phase detector (151).

Figure 2 is a block diagram about the symbol timing recovery apparatus of the present invention. Referring to Figure 2, as to the symbol timing recovery apparatus (142), by using the signal outputted

in the frequency downward device and matched filter (130), the signal is comprised of the timing error detector (210) detecting the timing phase difference, the integrator (230), the threshold value comparator (240), the timing phase controller (250) outputting the control signal controls so that the output of the comparison result integrator (230) of the threshold value comparator (240) select the coefficient group of the other interpolation filter in case of being greater than the threshold value and for removing the timing phase difference, and the reset circuit (220). The integrator (230) integrates the detected phase difference as described above until it reaches the standard threshold. The threshold value comparator (240) is integrated in the integrator (230) and compares the output value and threshold value. The reset circuit (220) controls in order to reset the threshold value in case of deviating from the fixation standard.

At this time, as to the control signal outputted in the timing phase controller (250), it selects the coefficient of the interpolation filter so that the symbol block be formed at the location which is inputted to the interpolation filter (141) and compensates for the output of the interpolation filter as the phase difference.

In the meantime, the timing error detector (210) adopted the decision-directed mode of the Gardner among the feedback loop mode of the various. This method is the method for detecting the symbol timing phase difference about the input signal by using the sampled-data at the sampled-data determined on the symbol timing and the spot having 1/2 difference in the symbol timing spot.

The error signal sharing with this and is detected is integrated in the integrator (230). And if the threshold value is exceeded, the signal integrated with the comparison result the of the threshold value comparator (240) is generated the control signal for operating a controller in the timing phase controller (250).

At this time, if the threshold value exceeds the standard value to the direction of an amount, the signal which is integrated while having an amount and negative value outputs the value of a +1 and the threshold value has the value smaller than the threshold value of a nagative, it outputs the value of -1. And it performs the function the threshold value selects the interpolation filter coefficient group used in the interpolation filter (141) in the symbol timing control circuit (250) by using this value and of controlling the symbol timing. In case the threshold value is a +1 or -1, it respects the value stored in an integrator with the reset (reset) below and the circuit added and subtracts as the threshold value is comprised in the reset circuit (220) according to an output.

Figure 3 is a process flow chart about the process of calculating the interpolation filter output according to the embodiment of the present invention. Figure 3 shows the process when it assumed the coefficient group of the interpolation filter which was currently selected in the output calculation of the interpolation filter to be N number coefficient group, of performing the selection of the filter coefficient group in the output calculation of the selection of the interpolation filter output, and out time and interpolation filter.

Referring to figs. 2 and 3, firstly, it is the case where the signal in which the control signal inputted to the timing control circuit is integrated with one person case (301) exceeds than the standard value to the direction of an amount. Therefore, if the interpolation filter coefficient group is the final filter coefficient group (302), the change (306), and interpolation filter output are delaid with the calculation (307) one Hoo, and the symbol fixed term sample and the interpolation filter coefficient group is to the first filter coefficient group the output (308). And if it is not interpolation filter coefficient group the final filter coefficient group (302), the change (303), and interpolation filter output are printed out to the previous filter coefficient group +1 number filter coefficient group with the calculation (304) and the interpolation filter coefficient group is in the symbol time the output (305).

It is the case where the signal in which the control signal inputted to the timing control circuit is integrated with -1 phosphorus case (309) exceeds than the standard value to the direction of the negative principle in nature. Therefore, if the interpolation filter coefficient group is the final filter coefficient group (310), the interpolation filter coefficient group is to the final filter coefficient group the

change (311) and the interpolation filter output is printed out with the calculation (312). And it precedes with the symbol fixed term sample and it does with the output (313). And presently, if it is not interpolation filter coefficient group the first filter coefficient group (310), the interpolation filter coefficient group the change (314), and interpolation filter output is printed out in the calculation (315) one Hoo, and the symbol time to the previous filter coefficient group - 1 number filter coefficient group with the output (316). 1 is not control signal inputted to the timing control circuit. If it is not -1, the interpolation filter coefficient group is to the previous filter coefficient group the establishment (317).

At this time, in the timing recovery circuit, the output of the interpolation filter outputs one sample to the symbol timing in one sample and 1/2 symbol timing since using the sample of 2 per a symbol.

Figure 4 is a drawing showing the form of the interpolation filter used for the symbol timing recovery. Referring to Figure 4, the coefficient (C which the interpolation filter is the value of necessary *** the inputted sample set up according to the coefficient group in the interpolation filter calculator (420) in advance 1 , C 2 , ..., C N-1 Hoo all values multiplying with the) (421) (422) are summed in the output device (430) and it outputs. At this time, as to the outputted signal, a signal is outputted when the symbol time time, the symbol time and phase difference are 1/2 for the symbol timing recovery. The timing error is detected in the timing error detector by using this value.

In case of the interpolation filter presented in above statement, this is used the half because the coefficient symmetrically shows up based on an origin. In that way the computational complexity and calculation time can be reduced. And figure 5 is a drawing about the interpolation filter of the present invention using a characteristic of such interpolation filter coefficient.

Referring to Figure 5, this interpolation filter has the folding structure. It add (520)s and it gives coefficients in which the coefficient group 1/2 is the coefficient group for calculating the interpolation filter since having the value which is a symmetric symmetrical about an origin before the use (530), the coefficient group and multiply. Thereafter, it multiplies with the signal selected with the control signal and the result of the whole is added (540) and the output of the interpolation filter is made. This configuration reduces to a complexity by 1/2. It reduces than the method presenting the circuit adding the signal outputted in each register or multiplies in fig. 4 by 1/2. In that way it reduces to the calculating speed and complexity and it shows the structure of being usable in the high-speed communications circuit.

Effects of the Invention

As to the present invention as described above, by using the interpolation filter which was usable in the high speed communication, it restored the symbol timing of the received signal in the base band. And the symmetry measure two values reduced to the complexity of the interpolation filter structure in the calculation of the interpolation filter by 1/2 by using as one. Moreover, the coefficient used in the interpolation filter of the present invention was chosen as the group of 4 and it had the resolution of a quadruple per a sample. It selected the coefficient of the interpolation filter with the symbol timing phase difference using the feedback loop. In that way it prevented the performance degradation even when ruling out the phase locked loop system.

Scope of Claims

Claim 1 :

The timing recovery device of the timing recovery device of the communications system using the interpolation filter, wherein it is comprised of the symbol timing recovery apparatus generated around the digital interpolation filter, which interpolates the input signal it is composed of the raised-cosine filter it prevents the timing slip generated in the A/D converter converting the received analog signal into a digital and the control signal preventing the timing slip to the digital interpolation filter.

Claim 2 :

The timing recovery device using the interpolation filter of claim 1, wherein: it is comprised of the timing error detector detecting the timing phase difference generated around the service clock difference of a transceiver, the integrator, the threshold value comparator, the timing phase controller outputting the control signal controls so that the output of the comparison result integrator of the threshold value comparator select the coefficient group of the other interpolation filter in case of being greater than the threshold value and for removing the timing phase difference to the digital interpolation filter, and the reset circuit; the integrator integrates the phase difference found from the timing error detector until it reaches the standard threshold; the threshold value comparator is integrated in an integrator and compares the output value and threshold value; and the reset circuit the symbol timing recovery apparatus controls in order to reset the threshold value in case the threshold value deviates from the fixation standard.

Claim 3 :

The timing recovery device using the interpolation filter of claim 1, wherein the digital interpolation filter has the folding structure; it sums the coefficient group before a signal and the received multiply with the symmetrical coefficient group since the coefficient group has the value which is a symmetric about an origin; and it multiplies with the signal selected with the control signal outputted in the symbol timing recovery apparatus and it adds and outputs the result of the whole.

Claim 4 :

The timing recovering method using the interpolation filter of the timing recovering method of the communications system using the interpolation filter, wherein comparing the integrated value of the first process, of saving the integrated value of the phase difference if the timing phase difference is generated due to the service clock difference of a transceiver and phase difference with the threshold value, a +1 is outputted to the control signal of the interpolation filter if the integrated value exceeds over the standard value to the direction of an amount; and the integrated value outputs the value of -1 if it is smaller than the threshold value of the negative principle in nature and it is comprised of the second process of outputting to the control signal of the interpolation filter, and the third process of the interpolation filter determining the output of the interpolation filter and output sample location of the interpolation filter in the second process with the control signal and performing the symbol timing recovery.

Claim 5 :

The timing recovering method using the interpolation filter of claim 4, wherein the selected coefficient group is N number; the control signal inputted to the timing control circuit restores the timing with 0 persons the interpolation filter; and the timing control circuit dismisses 0 to an output and an output is the coefficient of the interpolation filter comprised of the step that the second process controls, and the step that it controls in order to calculate the output of the interpolation filter with the selected coefficient group as described above and it lets the output signal go to the symbol time in order to use N number coefficient group.

Claim 6 :

The timing recovering method using the interpolation filter of claim 4, wherein the selected coefficient group is N number; the control signal inputted to the timing control circuit restores the timing with the +1 phosphorus interpolation filter; it examines whether whether the current interpolation filter coefficient group is the final filter coefficient group or not is not and or not it selects the coefficient group of the interpolation filter as the first coefficient group if it is the final filter coefficient group; and the output is comprised of the step that the second process controls, and the step that it controls in order to the interpolation filter coefficient select N+1 the filter coefficient group if be not final filter coefficient group and it calculates the output of the interpolation filter and it lets an output go to the

symbol time in order to the point of time when being delayed with one sample per a symbol dismiss an output after calculating the output of the interpolation filter.

Claim 7 :

The timing recovering method using the interpolation filter of claim 4, wherein the selected coefficient group is N number; the control signal inputted to the timing control circuit restores the timing with -1 phosphorus interpolation filter; and the output is comprised of the step that the second process controls, and the step that it controls in order to choose the previous N-1 number coefficient group in case be not coefficient group of the interpolation filter the first coefficient group and it calculates the output of the interpolation filter and it lets an output go to the symbol time so that it one sample previously discharge an output than the symbol sample time after it checks out whether the current interpolation filter coefficient group is the first coefficient group and or not it selects the coefficient group of the interpolation filter as the final filter coefficient group if it is the first coefficient group and calculating the output of the interpolation filter.

Drawings

Fig. 1

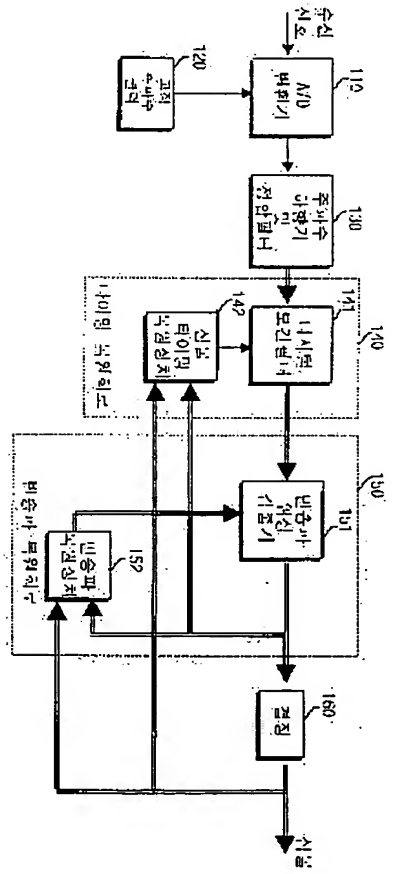

Fig. 2

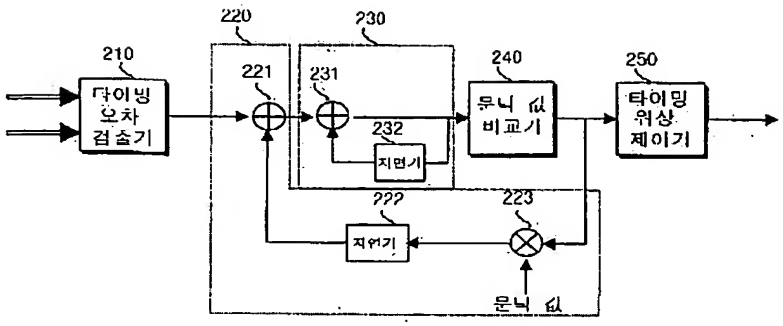

Fig. 3

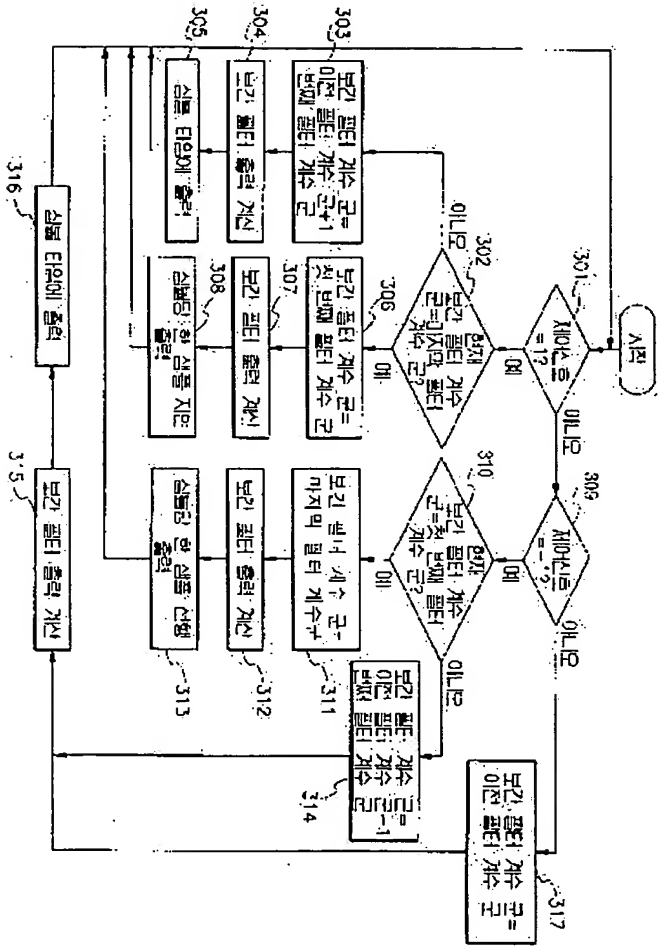

Fig. 4

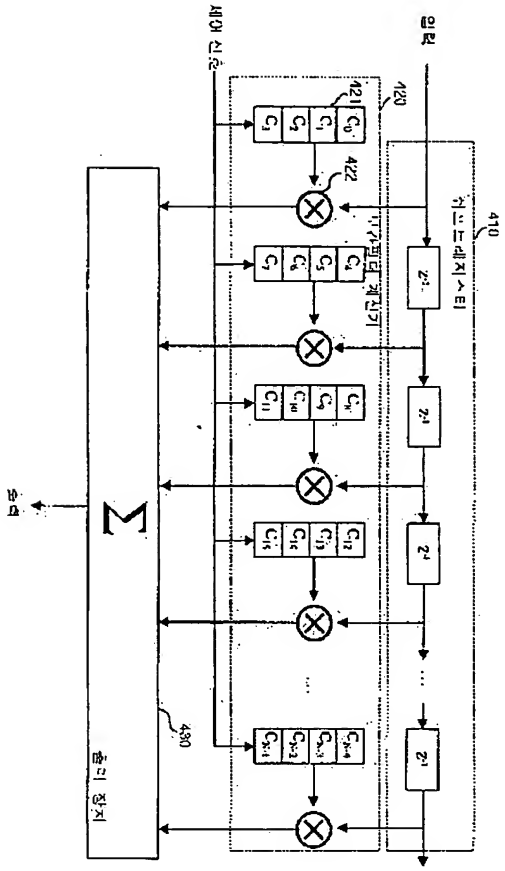

Fig. 5